AMENDMENT TO THE CLAIMS
Please replace the current version of the claims with the following rewritten version:

Listing of Claims:

1. (Currently Amended) An LCD apparatus comprising:

an LCD panel displaying images and including:

a first substrate;

a second substrate facing the first substrate, a plurality of pixels being provided on the second substrate;

a common electrode disposed on the first substrate;

gate lines disposed on the second substrate and opposing the common electrode, the gate lines receiving a gate driving signal;

data lines for supplying image data signals to the pixels; and

an output instruction signal line disposed on the second substrate and opposing the common electrode;

a data driver disposed on a data tape carrier package (TCP);

a gate driver outputting a gate driving signal to the LCD panel; and

a timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode, and depending on a resistive load ~~offormed by~~ the output instruction signal line ~~and the common electrode~~,

wherein the output instruction signal line is disposed between the data TCP and the gate lines, and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal.

2. (Previously presented) The LCD apparatus of claim 1, wherein the output instruction signal line is formed on an area adjacent to the data driver.

3. (Previously presented) The LCD apparatus of claim 2, further comprising a plurality of signal transmission members electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from the timing controller via one of the signal transmission members.

4. (Previously Presented) The LCD apparatus of claim 3, wherein the LCD panel comprises:

the gate lines receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction.

5. (Previously Presented) The LCD apparatus of claim 4, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines.

6. (Original) The LCD apparatus of claim 4, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines, and the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area.

7. (Currently Amended) An LCD apparatus comprising:

an LCD panel displaying images and including:

a first substrate;

a second substrate facing the first substrate, a plurality of pixels being provided on the second substrate;

a common electrode disposed on the first substrate;

gate lines disposed on the second substrate and opposing the common electrode, the gate lines receiving a gate driving signal;

data lines for supplying image data signals to the pixels; and

an output instruction signal line disposed on the second substrate and opposing the common electrode;

a data driver disposed on a data tape carrier package (TCP);

a gate driver outputting a gate driving signal to the LCD panel;

a timing controller providing a first control signal to the gate driver so as to control an output timing of the gate driving signal, and providing the output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode, and depending on a resistive load ~~offormed by~~ the output instruction signal line ~~and the common electrode~~; and

a plurality of signal transmission members electrically connecting the data driver with the LCD panel;

wherein the output instruction signal line provides the output instruction signal to the data driver via one of the signal transmission members;

wherein the output instruction line is disposed between the data TCP and the gate lines; and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed such that a delayed time of the image data signal is substantially equal to the delayed time of the gate driving signal.

8. (Previously Presented) The LCD apparatus of claim 7, wherein the LCD panel comprises:

the gate lines extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines extended in the second direction and arranged in the first direction.

9. (Previously presented) The LCD apparatus of claim 8, wherein the output instruction signal line is extended in the first direction.

10. (Original) The LCD apparatus of claim 9, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines, and the gate driving signal and the image data are substantially simultaneously provided to a corresponding pixel area.

11. (Previously Presented) The LCD apparatus of claim 7, wherein the output instruction signal line is formed on the LCD panel and adjacent to the data driver.

12. and 13. (Cancelled)

14. (Previously Presented) The LCD apparatus of claim 1, further comprising a plurality of signal transmission members electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from the timing controller via one of the signal transmission members.

15. (Previously Presented) The LCD apparatus of claim 1, wherein capacitive and resistive loads of the gate lines and the output instruction signal line are substantially equal to each other.

16. (Previously Presented) The LCD apparatus of claim 1, wherein a delay of providing the output instruction signal to the data driver is substantially equal to the delay of the gate driving signal.

17. (Previously Presented) The LCD apparatus of claim 1, wherein a portion of the output signal line is disposed on the data driver.